Sem - III - IT 2nd Half 2017
Sub - LD
Date - 29/11/2017

Q.P. Code: 24[illegible]

(3 Hours) [Total Marks: 80

N.B.: (1) Question No. 1 is **compulsory.**
(2) Solve any **three** questions out of remaining **five.**
(3) Figures to **right** indicate **full** marks.
(4) Assume suitable **data** where **necessary.**

Q1. Solve any four **20**
a) Prove that NOR gate is a universal gate.
b) Convert following decimal number to Binary ,Octal, Hexadecimal and Gray code $(2538)_{10}$
c) Derive relation between α and β.
d) Design full adder using half adder and additional gates.
e) Covert D flip flop to T flip flop.

Q2. a) Explain Voltage Divider Biasing Circuit with its stability factor. **10**
b) Using Quine MC Cluskey Method determine Minimal SOP form for **10**
$F(A,B,C,D)= \sum m(0,1,3,7,8,9,11,15)$

Q3. a) Implement following using only one 8:1 Multiplexer and few gates.
$F(A,B,C,D)= \sum m(0,1,3,4,5,7,9,10,12,15)$ **10**
b) With neat logic diagram explain operation of 4-bit Bidirectional Shift Register. **10**

Q4. a) Design a Mod 12 asynchronous counter using J-K Flipflop. **10**
b) Minimize the following four variable logic function using K-map **10**
i) $f(A,B,C,D)=\sum m(0,1,3,4,7,9,11,13,15)$
ii) $f(A,B,C,D)=\pi M(0,2,5,6,10,12,13,14)$

Q5. a) Simplify following equation using Boolean algebra and Design using basic gates **10**
i) $(A+B)(A+C)$
ii) $(A+C)(AD+\overline{AD})+AC+C$
b) Explain VHDL program format and write VHDL program for NAND gate. **10**

Q6 Solve any four- **20**
a) 3-bit binary to Gray code conversion.
b) Working of Master slave J-K flip flop.
c) Explain working Current Mirror Circuit.
d) Write VHDL program for Half Subtractor circuit.
e) Explain working of 3:8 Decoder.

(84) LD
SE/IT/Sem III/Choice
29/11/17.