(3 Hours) **[Total Marks: 80]**

N.B.: (1) Question No. 1 is **Compulsory**.
(2) Attempt any **three** questions out of **remaining five**.
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

1. Solve **any 4** of the following; (20)
   (a) Draw and explain AND gate using pass transistor logic (5)
   (b) Implement $Y = (A+B.C)$ using dynamic CMOS logic. (5)
   (c) Explain low power design consideration (5)
   (d) Implement half adder circuit using static CMOS. (5)
   (e) Draw schematic for 6T SRAM cell and explain its stability criteria (5)

2. (a) Explain concept of precharge and evolution in dynamic CMOS (10)
   (b) Define scaling? Explain various types of scaling in detail (10)

3. (a) Compare Ripple carry adder and carry-look-ahead adder. Explain 4 bit CLA adder implementation. (10)
   (b) Explain various techniques of clock generation. Discuss 'H' Tree clock distribution (10)

4. (a) Consider a CMOS inverter circuit with following parameter (10)
   $V_{Ton} = 0.6$ V, $V_{Top} = -0.7$V,
   $\mu_n Cox = 60\mu A/V^2$, $(W/L)_n = 8$
   $\mu_p Cox = 25\mu A/V^2$, $(W/L)_p = 12$

   Calculate noise margins and switching threshold of the inverter. The power supply voltage $V_{DD} = 3.3$V
   (b) Implement 4:1 MUX using pass transmission logic. Explain advantages of using transmission gates. (10)

5 (a) Explain Barrel shifter in brief. (10)
   (b) Draw JK flip flop using CMOS and explain its operation. (10)

6. Write short notes on **any two** of the following: (20)
   (a) ESD protection techniques
   (b) Interconnect scaling and crosstalk
   (c) Sense Amplifier
   (d) NAND based ROM array.